奇景光電股份有限公司
Himax Technologies, Inc.

HX8806 Data Sheet
TFT-LCD AV CONTROLLER

Preliminary Version 0.2

October, 2003

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DOC No:HX8806-17

HX8806

TFT-LCD AV CONTROLLER

PRELIMINARY

October, 2003, Version 0.2

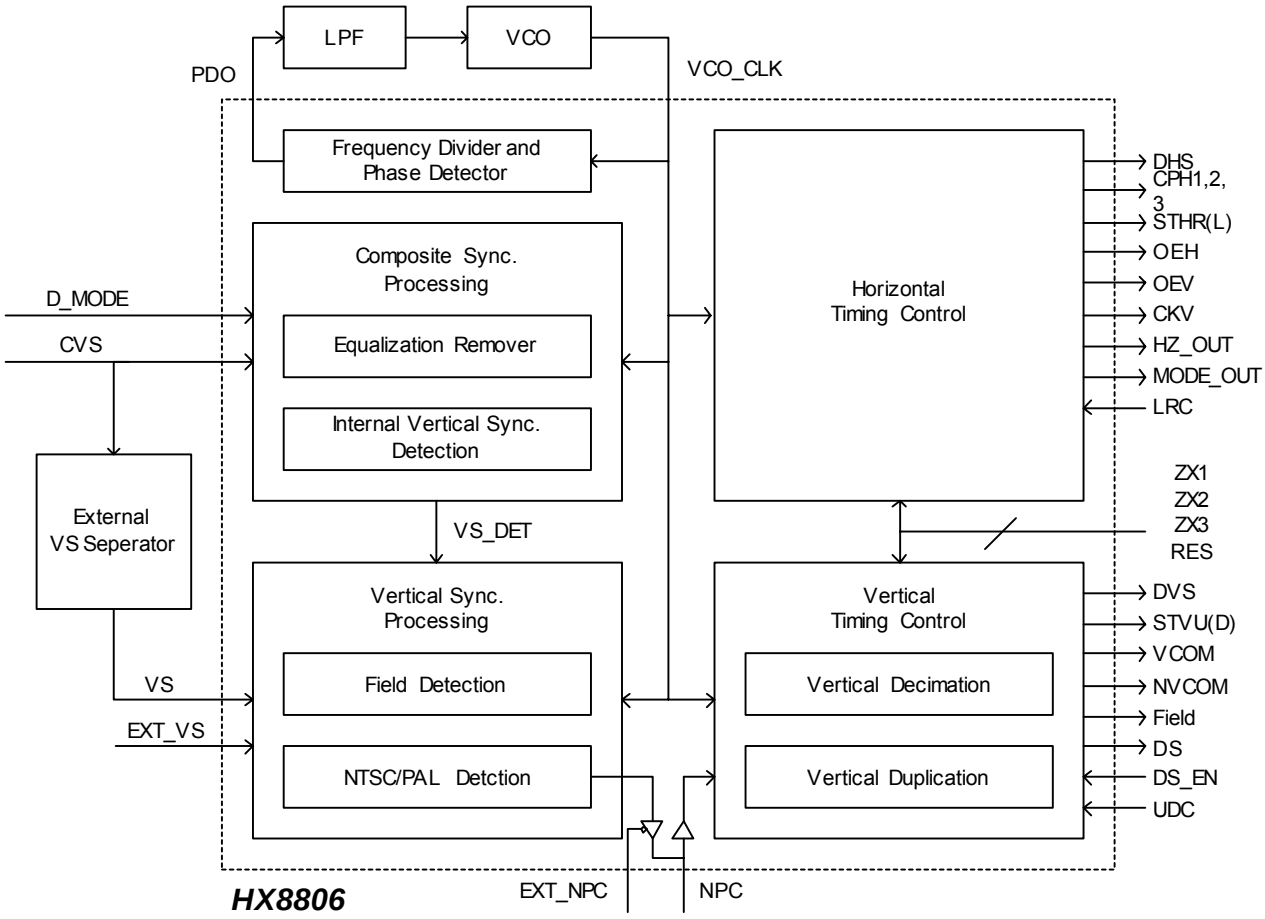
1. General Description

The HX8806 is a timing controller for small panel TFT-LCD. It provides horizontal and vertical control timing to TFT-LCD source and gate drivers. Built-in vertical synchronization detection circuit generates vertical synchronization signal internally without the extra components. Built-in phase lock loop sub-function with external VCO and low pass filter produces system clock which synchronizes input composite synchronization signal. HX8806 also provides 8 different zoom in/zoom out display modes for 2 different display resolutions.

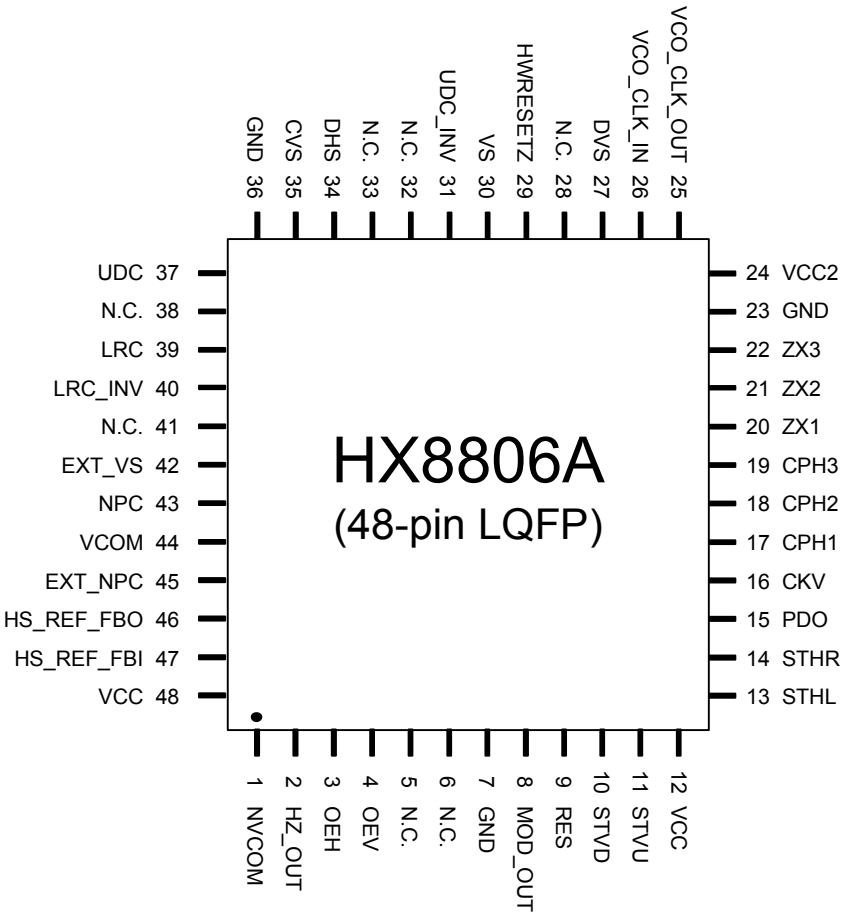
2. Features

- Programmable resolution mode.
- Master clock frequency: 30 MHz max.
- Built-in vertical sync. detection to omit the external sync. separator.
- Supply voltage: +5.0V or +3.3V.
- Shift clock signals for the source driver (3-ϕ Clock).
- Line inversion driving scheme.
- Support NTSC/PAL TV system.
- Provides control timings for source and gate drivers.
- Provides flip and mirror scan control.
- Built-in zoom in/zoom out display mode selection.
- 48 pins LQFP.

3. Block Diagram



4. Pin Assignment



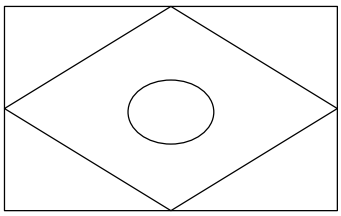
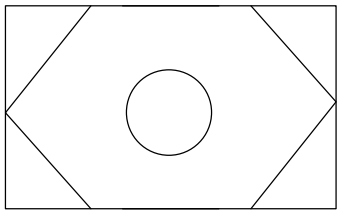
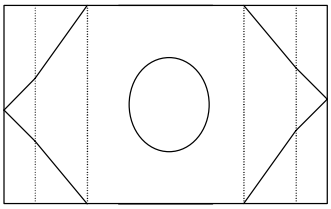
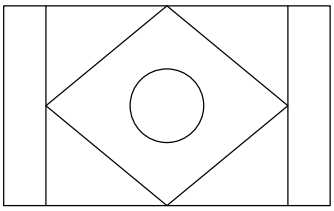
5. Pin Description

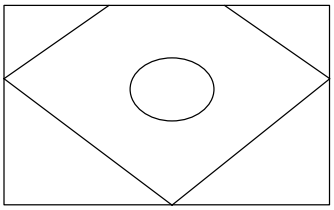
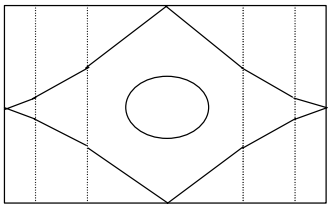
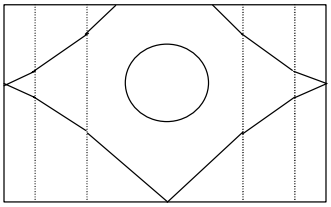
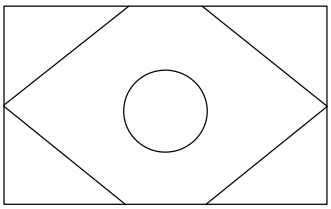
Pin no.	Symbol	I/O	Description
1	NVCOM	O	Inverter output of VCOM
2	HZ_OUT	O	Zoom in control signal
3	OEH	O	Source driver output enable control signal
4	OEV	O	Gate driver output enable control signal
5	N.C.		
6	N.C		
7	GND		Ground
8	MOD_OUT	O	Simultaneous/sequential sampling control setting of LCD.
9	RES	I	Resolution mode setting pin RES="H", 1440 resolution mode RES="L", 1200 resolution mode
10	STVD	O	Start pulse for gate driver. (1) STVD is "HiZ", when UDC="L" (2) STVD is "Output", when UDC="H"
11	STVU	O	Start pulse for gate driver. (1) STVU is "HiZ", when UDC="H" (2) STVU is "Output", when UDC="L"
12	VCC		Power for internal circuit
13	STHL	O	Start pulse for source driver. (1) STHL is "HiZ", when LRC="H" (2) STHL is "Output", when LRC="L"
14	STHR	O	Start pulse for source driver. (1) STHR is "HiZ", when LRC="L" (2) STHR is "Output", when LRC="H"
15	PDO	O	Phase detector output
16	CKV	O	Shift clock for gate driver
17	CPH1	O	Shift clock $\phi 1$ for source driver
18	CPH2	O	Shift clock $\phi 2$ for source driver
19	CPH3	O	Shift clock $\phi 3$ for source driver
20	ZX1(2)	I	Zoom in/out modes setting pin
21	ZX2(2)	I	Zoom in/out modes setting pin
22	ZX3(2)	I	Zoom in/out modes setting pin
23	GND		Ground
24	VCC2		Power for I/O pad
25	VCO_CLK_OUT	O	Inverted system clock signal output
26	VCO_CLK_IN	I	System clock input. It connects with external VCO and low pass filter circuits to generate system clock which synchronizes input composite synchronization signal
27	DVS	O	Negative polarity vertical synchronization signal output
28	DS	O	Dual scan mode vertical duplication control signal
29	HWRESETZ	I	Active low global reset signal input
30	VS	I	Negative polarity vertical synchronization signal

Pin no.	Symbol	I/O	Description
			input which is from the external synchronization separator circuits
31	UDC_INV	O	UDC inverted signal output
32	N.C.		
33	N.C.		
34	DHS	O	Horizontal synchronization signal output with negative polarity
35	CVS	I	Composite synchronization signal input with positive polarity
36	GND		Ground
37	UDC	I	Up / Down scan setting pin (1) Normal scan, when UDC="L" (2) Reverse scan, when UDC="H"
38	N.C		
39	LRC	I	Left / Right scan setting pin (1) Normal scan, LRC="L" (2) Reverse scan, LRC="H"
40	LRC_INV	O	LRC inverted signal output
41	N.C. (1)	O	Test pin
42	EXT_VS	I	VS detection setting pin (1) VS is from external detection , when EXT_VS="H" (2) VS is from internal detection , when EXT_VS="L"
43	NPC	I/O	Video signal input format setting pin; pull-up for normal operation.
44	VCOM	O	Toggling signal for common electrode generation circuits
45	EXT_NPC	I	NPC I/O setting pin (1) NPC is "Output", when EXT_NPC ="L" (2) NPC is "Input", when EXT_NPC ="H"
46	HS_REF_FBO	O	Reference signal output for phase lock loop operation
47	HS_REF_FBI	I	Reference signal input for phase lock loop operation
48	VCC		Power for internal circuit

Note: (1) The N.C. pins should be set "OPEN" for normal operation.

(2) Zoom in/out display mode setting:

Display Mode	ZX1	ZX2	ZX3	Display Characteristics (4:3 aspect-ratio input signal)	Remark
Full	H	H	H		Input signals are displayed on full screen.(To display 4:3 signal on 16:9 screen)
Zoom1	L	H	H		Central 176 lines of input signals are displayed on full screen. (Vertically extension, zoom factor =4/3).
zoom-Wide1	H	L	H		Central 176 lines of input signals are displayed on full screen. (Vertically extension and different horizontal timing scaling).
Normal	L	L	H		Input signal(4:3) are displayed on center 75% screen.(4:3 aspect-ratio).

Display Mode	ZX1	ZX2	ZX3	Display Characteristics (4:3 aspect-ratio input signal)	Remark
Zoom2	H	H	L		Lower 205 lines of input signals are displayed on full screen.(Zoom factor=8/7, vertically offset extension).
Wide	L	H	L		Input signals are displayed on full screen.(Different horizontal timing scaling).
Zoom-Wide2	H	L	L		Lower 205 lines of input signal are displayed on full screen. (Vertically extension and different horizontal timing scaling).
Zoom3	L	L	L		Center 205 lines of input signal are displayed on full screen. (Vertically extension, zoom factor=8/7).

6. DC Characteristics

6.1 Absolute maximum ratings:

Parameter	Symbol	Rating	Units
Power supply	V_{CC},V_{CC2}	-0.3 to 6.0	V
Input voltage	V_{IN}	-0.3 to V_{CC2} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC2} +0.3	V
Storage temperature	T_{STG}	-40 to 125	ºC

6.2 Recommended operating conditions:

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	V_{CC},V_{CC2}	3.0	5.0	5.5	V
Input voltage	V_{IN}	0	-	V_{CC}	V
Operating temperature	T_{OPR}	TBD	-	85	ºC

6.3 Electrical Characteristics:

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA
Tri-state leakage current	I_{OZ}		-10	-	10	μA
Input capacitance	C_{IN}		-	3	-	pF
Output capacitance	C_{OUT}		3	-	6	pF
Logic input low voltage	V_{IL}	CMOS	-	-	$0.3V_{CC2}$	V
Schmitt input low voltage	V_{SIL}(1)	CMOS	-	TBD	-	V
Logic input high voltage	V_{IH}	CMOS	$0.7V_{CC2}$	-	-	V
Schmitt input high voltage	V_{SIH}(1)	CMOS	-	TBD	-	V
Output low voltage	V_{OL}	I_{OL}=4mA	-	-	$0.2V_{CC2}$	V
Output high voltage	V_{OH}	I_{OH}=-4mA	$0.8V_{CC2}$	-	-	V
Input pull up/down resistance	R_I	V_{IL}= 0V or V_{IH}= V_{CC2}	50	-	100	kΩ

Note: (1) HWRESETZ, VCO_CLK_IN, VS, CVS, HS_REF_FBI.

6.4 Current consumption for 5 Volts operating:

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Full Chip Current Consumption	I_{IN}	Vcc=+5.0V, f_{OSC} = 23.2 MHz	-	14	21.5	mA
		Vcc=+5.0V, f_{OSC} = 29.1 MHz	-	16	23.5	mA

7. AC Characteristics

7.1 1440 mode

a. Input signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period		t_{OSC}	33	34	35	ns
CVS period		t_H	61.5	63.5	65.5	us
CVS pulse width		t_{CVS}	4	4.7	5.4	us
CVS rising time		t_{Cr}	-	-	700	ns
CVS falling time		t_{Cf}	-	-	300	ns
VS pulse width		t_{VS}	1	3	5	t_H
VS rising time		t_{Vr}	-	-	700	ns
VS falling time		t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC		-	262.5	-	line
	PAL		-	312.5	-	line

b. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time		t_r	-	-	10	ns
Falling time		t_f	-	-	10	ns
Clock high and low level pulse width		t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	$t_{CPH}/3$	-	ns
STH setup time		t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
DHS pulse width		t_{HS}	-	46	-	t_{CPH}
OEH pulse width		t_{OEH}	-	12	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	80	-	t_{CPH}
OEV pulse width		t_{OEV}	-	46	-	t_{CPH}
CKV pulse width		t_{CKV}	-	37	-	t_{CPH}
HS_REF_FBO period		t_{CP}	-	1	-	t_H
HS_REF_FBO pulse duty		t_{WCP}	-	1/2	-	t_H
DHS-OEH time		t_1	-	34	-	t_{CPH}
DHS-CKV time		t_2	-	28	-	t_{CPH}
DHS-OEV time		t_3	-	8	-	t_{CPH}
DHS-HS_REF_FBO time		t_4	-	32	-	t_{CPH}
STV setup time		t_{SUV}	-	16	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
DVS-STV time	NTSC	t_{VS1}	-	19	-	t_H
	PAL	t_{VS1}	-	27	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3

7.2 1200 mode

a. Input signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
VCO_CLK_IN period		t_{OSC}	40.3	41.6	43	ns
CVS period		t_H	61.5	63.5	65.5	us
CVS pulse width		t_{CVS}	4	4.7	5.4	us
CVS rising time		t_{Cr}	-	-	700	ns
CVS falling time		t_{Cf}	-	-	300	ns
VS pulse width		t_{VS}	1	3	5	t_H
VS rising time		t_{Vr}	-	-	700	ns
VS falling time		t_{Vf}	-	-	1.5	us
Horizontal lines per field	NTSC		-	262.5	-	line
	PAL		-	312.5	-	line

b. Output signal characteristics

PARAMETER		Symbol	Min.	Typ.	Max.	Unit.
Rising time(1)		t_r	-	-	10	ns
Falling time(1)		t_f	-	-	10	ns
Clock high and low level pulse width(2)		t_{CPH}	-	3	-	t_{OSC}
Clock pulse duty		t_{CWH}	40	50	60	%
3-ϕ clock phase difference		t_{C12}, t_{C23}, t_{C31}	-	$t_{CPH}/3$	-	ns
STH setup time		t_{SUH}	-	$t_{CPH}/2$	-	t_{CPH}
STH pulse width		t_{STH}	-	1	-	t_{CPH}
DHS pulse width		t_{HS}	-	36	-	t_{CPH}
OEH pulse width		t_{OEH}	-	9	-	t_{CPH}
Sample & hold disable time		t_{DIS1}	-	61	-	t_{CPH}
OEV pulse width		t_{OEV}	-	40	-	t_{CPH}
CKV pulse width		t_{CKV}	-	50	-	t_{CPH}
HS_REF_FBO period		t_{CP}	-	1	-	t_H
HS_REF_FBO pulse WIDTH		t_{WCP}	-	1/2	-	t_H
DHS-OEH time		t_1	-	27	-	t_{CPH}
DHS-CKV time		t_2	-	14	-	t_{CPH}
DHS-OEV time		t_3	-	12	-	t_{CPH}
DHS-HS_REF_FBO time		t_4	-	26	-	t_{CPH}
STV setup time		t_{SUV}	-	8	-	t_{CPH}
STV pulse width		t_{STV}	-	1	-	t_H
DVS-STV	NTSC	t_{VS1}	-	19	-	t_H
	PAL	t_{VS1}	-	27	-	t_H

Note: (1) For all of the logic signals.
(2) CPH1~3

7.3 Zoom in/out display mode

7.3.1 1440 mode

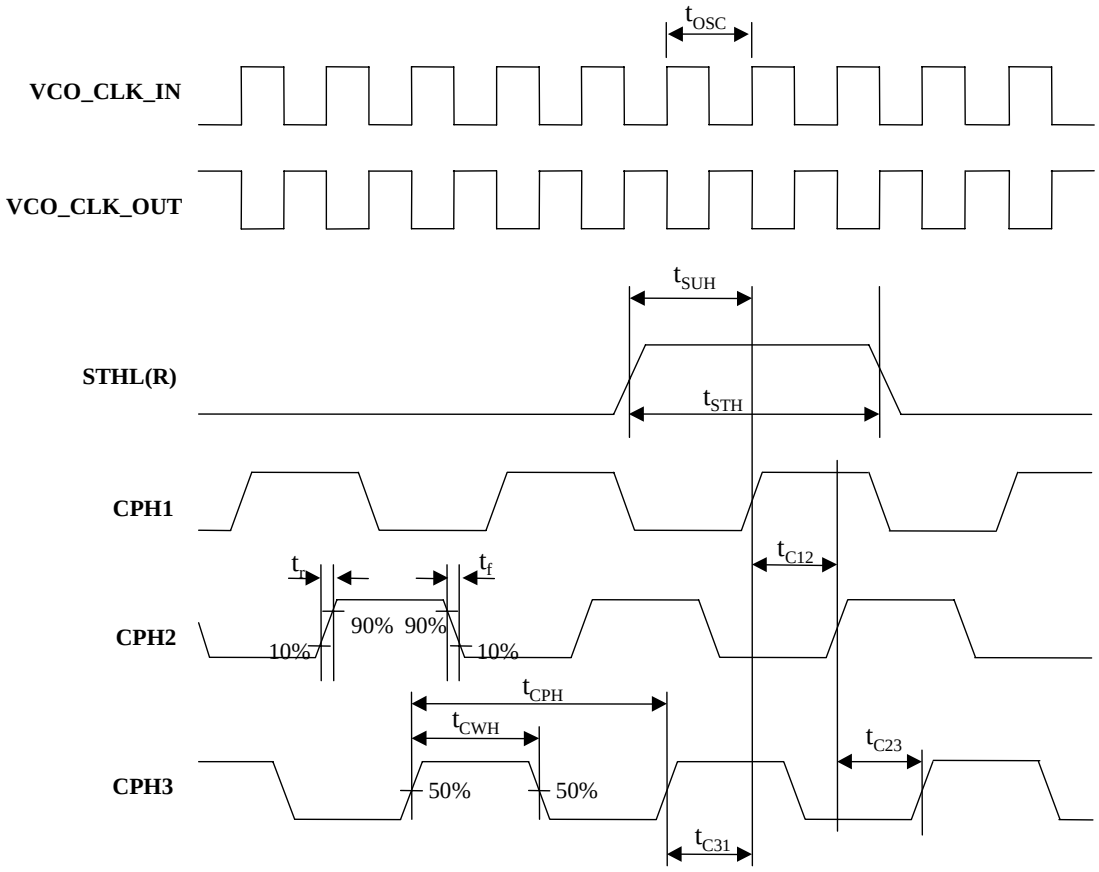
Zoom mode			Horizontal Display Start	Vertical Display Start
ZX1	ZX2	ZX3		
L	L	L	12.94us	33H
H	L	L	12.98us	45H
L	H	L	12.98us	19H
H	H	L	12.94us	45H
L	L	H	8.83us	19H
H	L	H	12.98us	48H
L	H	H	12.94us	48H
H	H	H	12.94us	19H
Remark			From falling edge of DHS to rising edge of STHL(R)	From falling edge of DVS to rising edge of STVU(D)

7.3.2 1200 mode

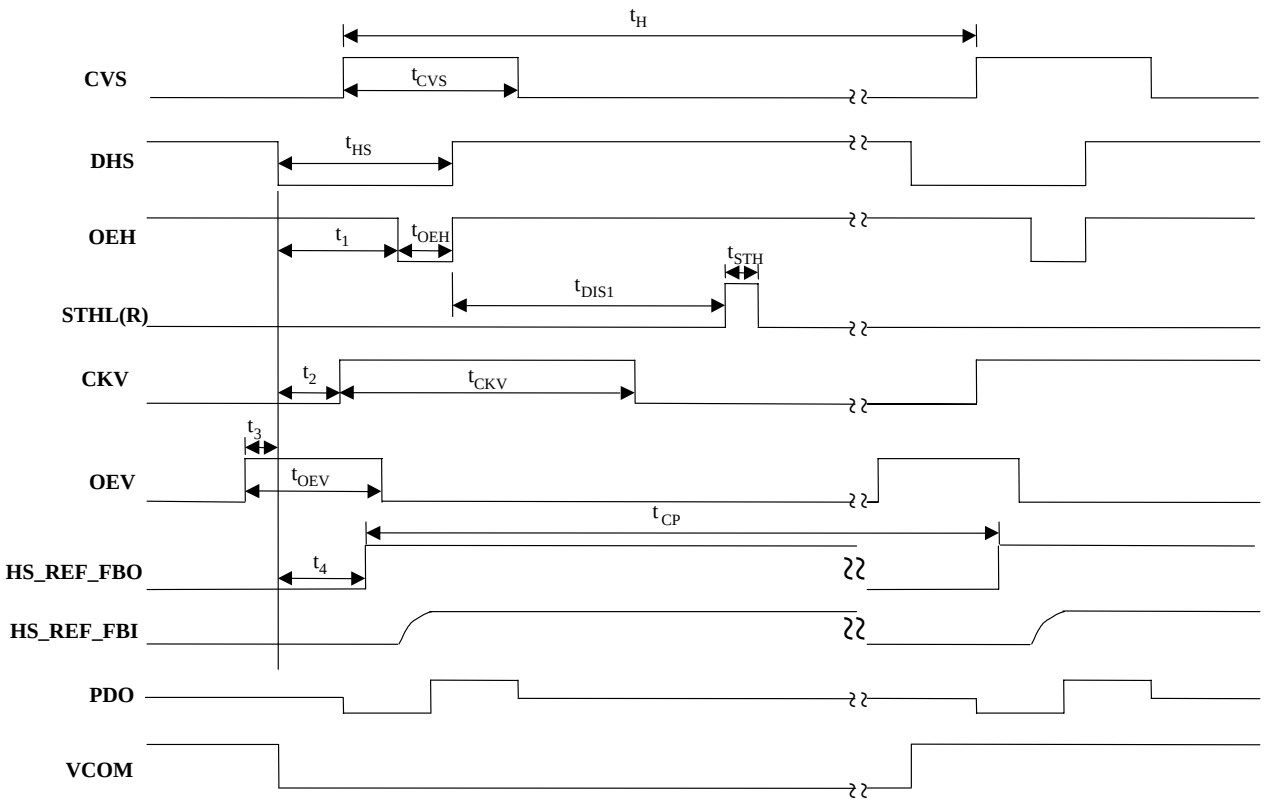
Zoom mode			Horizontal Display Start	Vertical Display Start
ZX1	ZX2	ZX3		
L	L	L	12.59us	33H
H	L	L	12.65us	45H
L	H	L	12.65us	19H
H	H	L	12.59us	45H
L	L	H	8.65us	19H
H	L	H	12.65us	48H
L	H	H	12.59us	48H
H	H	H	12.59us	19H
Remark			From falling edge of DHS to rising edge of STHL(R)	From falling edge of DVS to rising edge of STVU(D)

8. Waveform

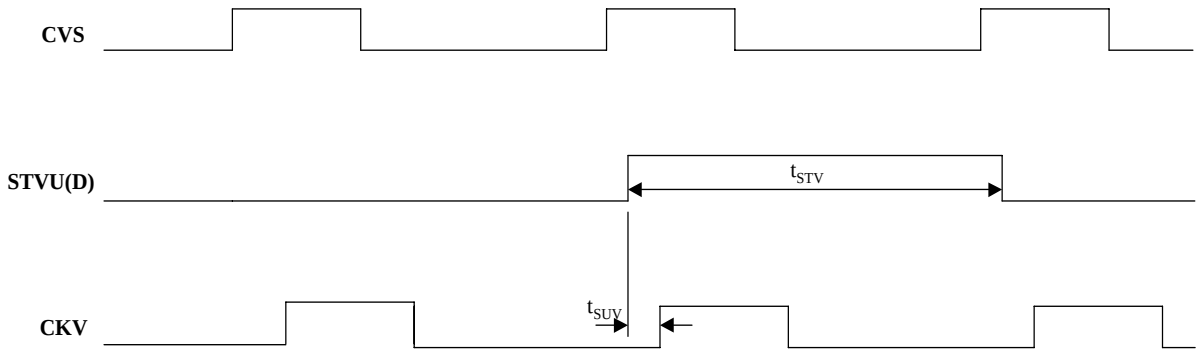
8.1 VCO_CLK, STHL(R) and CPH1~3 timing waveform



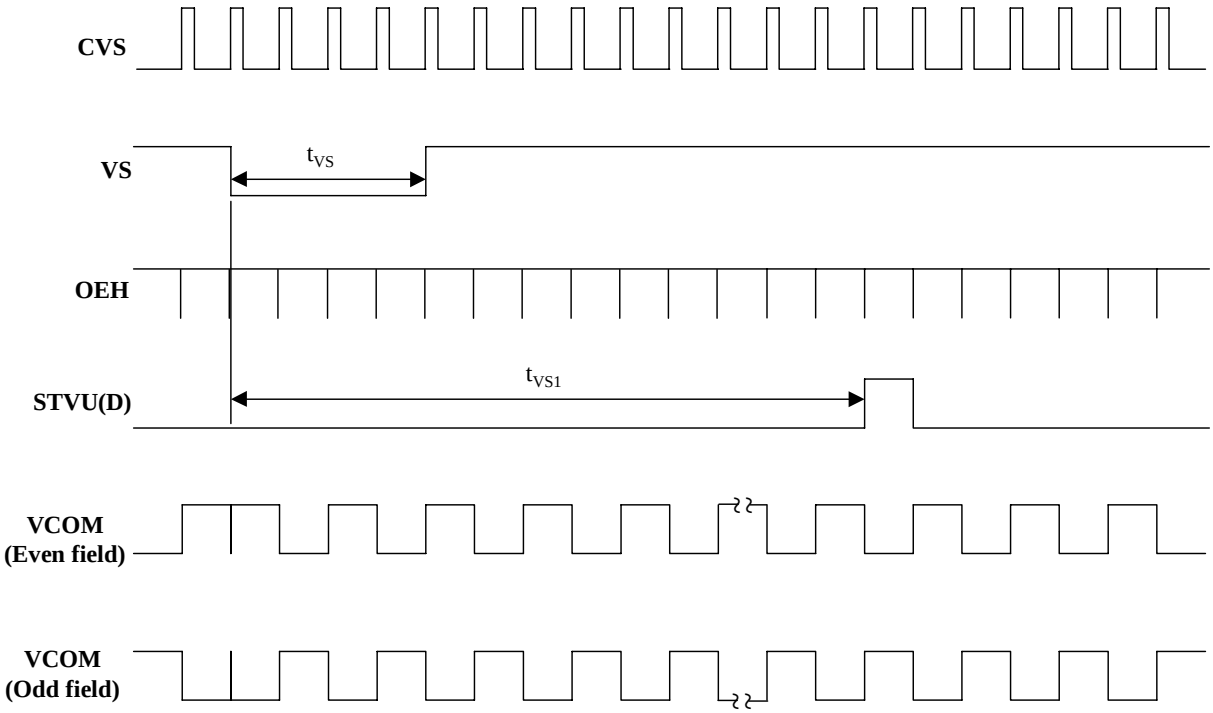
8.2 CVS and horizontal control timing waveform



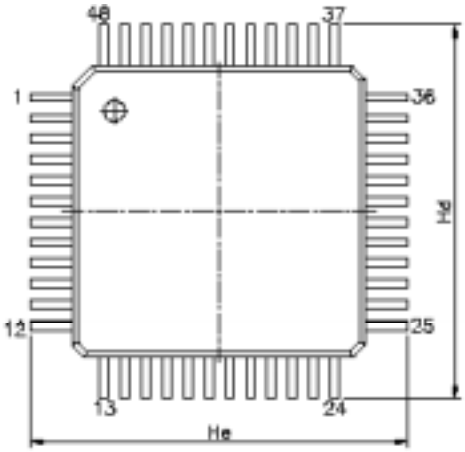
8.3 CVS and vertical shift clock timing waveform

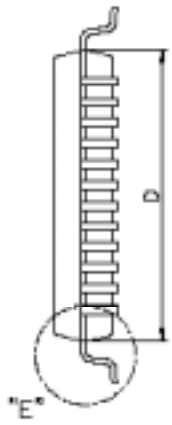


8.4 CVS and vertical control timing waveform



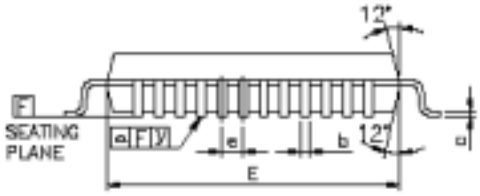
9. Package Outline Dimension

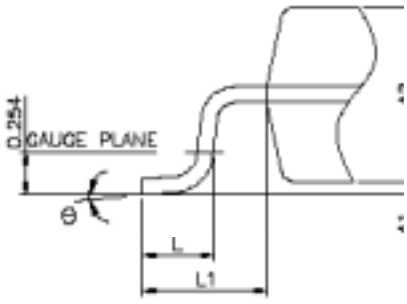




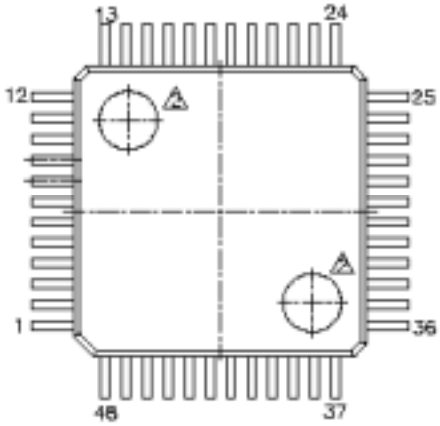
Symbol \ Unit	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400±0.05	0.0551±0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D	7.000±0.100	0.2756±0.0039
E	7.000±0.100	0.2756±0.0039
e	0.500TYP	0.0196TYP
Hd	9.000±0.250	0.3543±0.0098
He	9.000±0.250	0.3543±0.0098
L	0.600±0.150	0.0236±0.006
L1	1.000REF	0.0393REF
y	0.100MAX.	0.0039MAX.
θ	0°~7°	0°~7°

NOTES:
1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
3. MAX. END FLASH IS 0.15MM.
4. MAX. DAMBAR PROTRUSION IS 0.13MM.
5. GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.





DETAIL "E"



10. Ordering Information

Part NO.	Package
HX8806LA	48-pin LQFP

11. Revision History

Version	EFF.DATE	DESCRIPTION OF CHANGES
0.1	2003/06/03	New setup
0.2	2003/10/31	Update and modify